

REMARKS

Reconsideration of this application as amended is respectfully requested. Claims 1-49 stand rejected under 35 U.S.C. §112 First Paragraph. The Examiner has stated that

According to common usage a cell is a fixed length unit of transmission used by ATM. The word "cell" is therefore used to describe a unit of transmission rather than a property of a buffer. Applicant fails to define "cell" as it pertains to a description of the buffers. The disclosure therefore does not enable one of ordinary skill in the art to either make or use the invention.

(p. 2 Office Action 10/24/00).

The Applicant has amended the claims by replacing "cell" with "fixed-length transmission unit." The change results in no new matter being introduced. Support for the amendment is found in the specification at points where cells are discussed. For example, on page 15, line 22, the specification states that

The CBC interface uses a 16-bit data path that transmits cells that each comprise twenty-seven 16-bit words. **Figure 8** is a cell format of the QE mode of one embodiment.

(p. 15, line 22-24, Specification, 6/3/98). Later, on page 16, line 1, the specification states

In supporting the ATM mode, one CBC interface receive slave port and one CBC interface transmit slave port are used, but the embodiment is not so limited. The CBC interface comprises an 8-bit datapath that transmits cells that each comprise 56 byte words.

(p. 16, line 1-4, Specification, 6/3/98). While the length of a cell is fixed once in use, the length can be programmed to different sizes depending on the system being interfaced with and other factors. The cited example shows a cell of one

fixed length to meet the requirements, such as headers, for a QE interface and a second fixed length to meet the requirements for an ATM transmission.

Claims 23 and 24 stand rejected under 35 U.S.C. §112 second paragraph as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention. Specifically, the Examiner states, "It is therefore unclear to which of the unidirectional FIFO buffers the term 'the write port cell count' is intended to refer in claims 23 and 24." Applicants have amended Claims 23 and 24 to clarify the matter.

Claims 34-41 are rejected under 35 U.S.C. 112, second paragraph, as failing to set forth the subject matter which the Applicants regard as their invention. The Examiner states that

Claim 34 recites "A network switch platform comprising ... at least one discard enable signal." It is obvious to one of ordinary skill in the art that a network platform cannot comprise a signal. Claims 35-41 depend on claim 34 and are thus similarly rejected.

(p. 4, Office Action 10/24/00). Applicants have amended Claim 34 to clarify the matter. As Claims 35-41 were rejected as being dependant on Claim 34, the clarification of Claim 34 extends to Claims 35-41.

Claims 1-3, 20-22, 25-32, 42-45, 47, and 48 are rejected under 35 U.S.C. 103(a) as being unpatentable over U.S. Patent No. of 5, 940,368 of Takamichi et al. (Takamichi) in view of U.S. Patent No. 5,406,554 of Parry (Parry). The Examiner states that

With regard to claims 1, 3, 42, and 43, Takamichi et al. discloses an apparatus comprising at least one bidirectional FIFO unit, wherein each such bidirectional FIFO unit comprises a first and second unidirectional FIFO buffer (Fig. 6; column 6, lines 28-32; cell buffer pairs 51—55, 7-8, and 61-61). As discussed above, the limitation that a cell size of each of the FIFO buffers is programmable is interpreted in what follows to mean that

the word size of each of the FIFO buffers is programmable. Takamichi et al. fails to disclose an invention for which the buffer word size is programmable. Parry teaches a FIFO buffer that is useful ATM applications and whose word size can be programmed by either using more than one FIFO or varying the width of the input data bus (Fig. 3; column 13, lines 23-39). It would have been obvious to one of ordinary skill in the art to modify the invention of Takamichi et al. so that the word size of each of the FIFO buffers is programmable, as in Parry, because such a modification allows the invention to be used on a larger number of servers because servers vary in the word size they handle.

(p. 5-6, Office Action 10/24/00).

First, in this passage, the Examiner characterizes cell size to be the equivalent of word size. Earlier in the office action, the Examiner had stated, "This statement defines 'cell size' as it pertains to the buffer as being the 'number of words per cell.'" (p. 2 Office Action 10/24/00).

Secondly, Applicants respectfully submit that Claims 1 and 42 are not obvious under Takamichi in view of Parry. Claim 1 discloses the limitation, "wherein a fixed-length transmission unit size of the first and second unidirectional FIFO buffers is programmable." (Claim 1)(emphasis added). Claim 42 discloses the limitation, "wherein the bidirectional FIFO unit comprises a first and a second unidirectional FIFO buffer having a programmable fixed-length transmission unit size." (Claim 42)(emphasis added).

In contrast, neither Takamichi nor Parry disclose the fixed-length transmission unit size of the first and second unidirectional FIFO buffers is programmable. The Examiner admits Takamichi contains no such limitation. Parry discloses that

With reference now to FIG. 3, an expanded width FIFO 76 is shown. Expanded width FIFO 76 incorporates two FIFOs 10 as previously described with respect to FIG. 1. Further, with respect to expanded width FIFO 76 as illustrated in FIG. 3, like structure to that above-described with

respect to FIG. 1 is like numbered, and the foregoing description thereof shall suffice herefor.

In the example shown in FIG. 3, two input data buses 14 may be combined to a width of 18 bits or to any multiples of 8 or 9 as may be required. Utilizing the dual write and read enable signals of FIFO 10, along with separate count down clocks, data from an 8 or 9 bit bus can be stored in whatever width desired, and then re-interleaved back into an 8 or 9 bit format on output data buses 64 to allow the use of slower FIFO's 10 on fast data buses.

(Parry, Col. 13, lines 23-39). Parry discloses physically varying the size of the FIFO memory capacity.

Given that claims 2-33 depend from claim 1 and claims 43-49 depend from claim 42, and the above limitation fails to appear in the other cited references, applicants submit that claims 2-33 and 43-49 are not anticipated under 35 U.S.C. §103(a) by the reference cited by the Examiner.

It is respectfully submitted that in view of the amendments and arguments set forth herein, the applicable rejections and objections have been overcome.

If there are any additional charges, please charge Deposit Account No. 02-2666.

Respectfully submitted,

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VERSION WITH MARKINGS TO SHOW CHANGES MADE

IN THE CLAIMS

Please amend the claims as follows:

1. An apparatus for controlling fixed-length transmission unit traffic in a switch platform, the apparatus comprising at least one bi-directional first-in-first-out (FIFO) unit,

Wherein each bi-directional FIFO unit comprises a first and a second unidirectional FIFO buffer, wherein a fixed-length transmission unit size of the first and second unidirectional FIFO buffers is programmable.

2. The apparatus of claim 1, wherein the first and second unidirectional FIFO buffers each comprise asynchronous read and write ports.

3. The apparatus of claim 1, wherein a word size of the first and second unidirectional FIFO buffers is programmable.

4. The apparatus of claim 1, wherein the at least one bi-directional FIFO unit is coupled to write at least one fixed-length transmission unit from and read at least one fixed-length transmission unit to at least one asynchronous transfer mode (ATM)

interface, at least one frame relay interface, at least one voice interface, and at least one data interface.

5. The apparatus of claim 1 wherein the first unidirectional FIFO buffer is coupled to write at least one fixed-length transmission unit from an ATM interface.

6. The apparatus of claim 1, wherein the first unidirectional FIFO buffer is coupled to write at least one fixed-length transmission unit from a relay interface.

7. The apparatus of claim 1, wherein the first unidirectional FIFO buffer is coupled to write at least one fixed-length transmission unit from a voice interface.

1 8. The apparatus of claim 1, wherein the first unidirectional FIFO buffer is
2 coupled to write at least one fixed-length transmission unit from a data
3 surface.

4

5 9. The apparatus of claim 1, wherein the first unidirectional FIFO buffer
6 is coupled to read at least one fixed-length transmission unit to at least one
7 switch, wherein the at least one switch handles fixed-length transmission
8 units from sources having a plurality of bandwidths.

9

10 10. The apparatus of claim 9, wherein the at least one switch is coupled
11 to route the at least one fixed-length transmission unit to an OC12 trunk line
12 and to at least one service module.

13

14 11. The apparatus of claim 10 wherein the at least one service module is
15 coupled to provide the at least one fixed-length transmission unit to at least
16 one service subscriber using T1, E1, T3, E3, OC3, and OC 12 ports.

17

18 12. The apparatus of claim 1, wherein the second unidirectional FIFO
19 buffer is coupled to read at least one fixed-length transmission unit
20 to an ATM interface.

21

22 13. The apparatus of claim 1, wherein the second unidirectional FIFO
23 buffer is coupled to read at least one fixed-length transmission unit to a
24 frame relay interface.

25

26 14. The apparatus of claim 1, wherein the second unidirectional FIFO
27 buffer is coupled to read at least one fixed-length transmission unit to a
28 voice interface.

29

30 15. The apparatus of claim 1, wherein the second unidirectional FIFO
31 buffer is coupled to read at least one fixed-length transmission unit to a data
32 interface.

33

34 16. The apparatus of claim 1, wherein the second unidirectional FIFO
35 buffer is coupled to write at least one fixed-length transmission unit from at
36 least one switch wherein the at least one switch handles fixed-length
37 transmission units from sources having a plurality of bandwidths.

38

39 17. The apparatus of claim 16, wherein the at least one switch is coupled
40 to route the at least one fixed-length transmission unit from an OC12 trunk
41 line and from at least one service module.

42

43 18. The apparatus of claim 17, wherein the at least one service module is
44 coupled to provide the at least one fixed-length transmission unit to at least
45 one service subscriber using T1, E1, T3, E3, OC3, and OC 12 ports.

46

47 19. The apparatus of claim 1, wherein the at least one bi-directional FIFO
48 unit comprises a diagnostic interface, wherein the diagnostic interface
49 supports a non-destructive read of the at least one bi-directional FIFO unit
50 while at least one fixed-length transmission unit is being written to and read
51 from the at least one bi-directional FIFO unit.

52

53 20. The apparatus of claim 1, wherein the at least one fixed-length
54 transmission unit is written to the second unidirectional FIFO buffer from the
55 first unidirectional FIFO buffer over a first enabled diagnostic loop.

56

57 21. The apparatus of claim 1, wherein the at least one fixed-length
58 transmission unit is written to the first unidirectional FIFO buffer from the
59 second unidirectional FIFO buffer over a second enabled diagnostic loop.

60

61 22. The apparatus of claim 1, wherein each unidirectional FIFO buffer
62 outputs a write port fixed-length transmission unit count, wherein a write
63 port of each unidirectional FIFO buffer outputs a status indicating space
64 available in the unidirectional FIFO buffer for at least one more fixed-length
65 transmission unit.

66

67 23. The apparatus of claim 22, wherein at least one master bi-directional
68 FIFO unit ceases reading at least one fixed-length transmission unit to the
69 first unidirectional FIFO buffer of at least one slave bi-directional FIFO unit
70 in response to write port fixed-length transmission unit count of the first
71 unidirectional FIFO buffer, wherein the at least one master bi-directional
72 FIFO unit disables at least one switch from routing at least one fixed-length
73 transmission unit to the at least one slave bi-directional FIFO unit in
74 response to the write port fixed-length transmission unit count, wherein the
75 at least one switch routes the at least one fixed-length transmission unit to
76 another of the at least one slave bi-directional FIFO units in response to the
77 write port fixed-length transmission unit count of the first unidirectional
78 FIFO buffer.

79

80 24. The apparatus of claim 23, wherein the at least one master bi-
81 directional FIFO unit resumes reading the at least one fixed-length
82 transmission unit to the second unidirectional FIFO unit resumes reading the
83 at least one fixed-length transmission unit to the second unidirectional FIFO
84 buffer of the at least one slaved bi-directional FIFO unit in response to the
85 write port fixed-length transmission unit count of the second unidirectional
86 FIFO buffer, wherein the at least one master bi-directional FIFO unit enables
87 at least one switch to route at least one fixed-length transmission unit to the
88 at least one slave bi-directional FIFO unit in response to the write port fixed-
89 length transmission unit count of the second unidirectional FIFO buffer.

90

91 25. The apparatus of claim 1, wherein each unidirectional FIFO buffer
92 outputs a read port fixed-length transmission unit count, wherein a read port
93 of each unidirectional FIFO buffer outputs a status indicating space available
94 in the unidirectional FIFO buffer for at least one more fixed-length
95 transmission unit.

96

97 26. The apparatus of claim 2, wherein the write port logic of each
98 unidirectional FIFO buffer is synchronous with the write clock.

99

100 27. The apparatus of claim 26, wherein the write clock operates at a
101 frequency substantially equal to 50 megahertz.

102

103 28. The apparatus of claim 26, wherein the read port logic of each

104 unidirectional FIFO buffer is synchronous with a read clock.

105

106 29. The apparatus of claim 28, wherein the read clock operates at a

107 frequency substantially equal to 21 megahertz.

108

109 30. The apparatus of claim 28, wherein the read clock operates at a

110 frequency substantially equal to 42 megahertz.

111

112 31. The apparatus of claim 1 wherein at least one invalid fixed-length

113 transmission unit can be discarded from each unidirectional FIFO

114 buffer.

115

116 32. The apparatus of claim 1, wherein the switch platform comprises two

117 switches.

118

119 33. The apparatus of claim 1, wherein the switch platform comprises at

120 least one service module and at least one fixed-length transmission

121 unit bus controller, wherein the at least one fixed-length transmission

122 unit bus controller is coupled among the at least one service module

123 and a least one switch, wherein the at least one service module

124 comprises at least one slave bi-directional FIFO unit, and wherein the

125 at least one fixed-length transmission unit bus controller comprises
126 at least one master bi-directional FIFO unit.

127

128 34. A network switch platform comprising:
129 at least one service module;
130 at least one fixed-length transmission unit bus controller
131 coupled among the at least one service module and at least one
132 switch;
133 at least one bi-directional first-in-first-out (FIFO) unit located
134 in the at least one service module and the at least one fixed-length
135 transmission unit bus controller, wherein each bi-directional FIFO
136 unit comprises a first and a second unidirectional FIFO buffer,
137 wherein a fixed-length transmission unit size of the first and second
138 unidirectional FIFO buffers is programmable;
139 at least one diagnostic interface, wherein the at least one
140 diagnostic interface supports a non-destructive read of the at least one
141 bi-directional FIFO unit while at least one fixed-length transmission
142 unit is being written to and read from the at least one bi-directional
143 FIFO unit; and
144 at least one discard enable signal input to the at least one
145 bidirectional FIFO unit, wherein at least one invalid fixed-length
146 transmission unit can be discarded from the at least one bi-directional

147 FIFO unit upon receiving a discard enable signal via the at least one
148 discard enable signal input.

149

150 35. The network switch platform of claim 34, wherein the at least one
151 bi-directional FIFO unit is coupled to write at least one fixed-length
152 transmission unit from and read at least one fixed-length
153 transmission unit to at least one asynchronous transfer mode (ATM)
154 interface, at least one frame relay interface, at least one voice
155 interface, and at least one data interface.

156

157 36. The network switch platform of claim 34, wherein the at least
158 one fixed-length transmission unit is written to the second
159 unidirectional FIFO buffer from the first unidirectional FIFO
160 buffer over a first enabled diagnostic loop, wherein at least one
161 fixed-length transmission unit is written to the first
162 unidirectional FIFO buffer from the second unidirectional FIFO
163 buffer over a second enabled diagnostic loop.

164

165 37. The network switch platform of claim 34, wherein each
166 unidirectional FIFO buffer outputs a write port fixed-length
167 transmission unit count, wherein a write port of each
168 unidirectional FIFO buffer outputs a status indication space
169 available in the unidirectional FIFO buffer for at least one more

170 fixed-length transmission unit, wherein each unidirectional
171 FIFO buffer outputs a read port fixed-length transmission unit
172 count, wherein a read port of each unidirectional FIFO buffer
173 outputs a status indicating space available in the unidirectional
174 FIFO buffer for at least one more fixed-length transmission
175 unit.
176
177

177 38. The network switch platform of claim 34, wherein the first and
178 second unidirectional FIFO buffers each comprise
179 asynchronous read and write ports, wherein the write port
180 logic of each unidirectional FIFO buffer is synchronous with a
181 write clock, and wherein the read port logic of each
182 unidirectional FIFO buffer is synchronous with a read clock.

183

184 39. The network switch of claim 34, wherein a word size of the
185 first and second unidirectional FIFO buffers is programmable.

186

187 40. The network switch platform of claim 34, wherein the at least one
188 bi-directional FIFO unit is coupled to read at least one fixed-
189 length transmission unit to and write at least one fixed-length
190 transmission unit from the least one switch, wherein the switch
191 handles fixed-length transmission units from sources having a
192 plurality of bandwidths.

193

194 41. The network switch platform of claim 34, wherein the at least
195 one service module is coupled to receive at least one fixed-
196 length transmission unit from and provide at least one fixed-
197 length transmission unit to at least one service subscriber using
198 T1, E1, T3, E3, OC3, and OC 12 ports.

199

42. A method for controlling fixed-length transmission unit traffic in a switch platform, the method comprising the step of transferring at least one fixed-length transmission unit among a plurality of ports having a plurality of bandwidths using a bi-directional first-in-first-out (FIFO) unit, wherein the bi-directional FIFO unit comprises a first and second unidirectional FIFO buffer having a programmable fixed-length transmission unit size.
43. The method of claim 42, further comprising the step of programming the word size of each of the first and second unidirectional FIFO buffers.
44. The method of claim 43, wherein the step of transferring comprises the steps of:
 - synchronously writing the at least one fixed-length transmission unit from at least one port to the first unidirectional FIFO buffer; and
 - synchronously reading the at least one fixed-length transmission unit from the first unidirectional FIFO buffer to at least one switch, wherein the reading is asynchronous with the writing.

45. The method of claim 42, wherein the step of transferring comprises the steps of:

synchronously writing the at least one fixed-length transmission unit from at least one switch to the second unidirectional FIFO buffer; and

synchronously reading the at least one fixed-length transmission unit from the second unidirectional FIFO buffer to the at least one port, wherein the reading is asynchronous with the writing.

46. The method of claim 42, further comprising steps of:

discarding at least one invalid fixed-length transmission unit from each unidirectional FIFO buffer; and

executing a non-destructive read of the at least one bi-directional FIFO unit while at least one fixed-length transmission unit is being written to and read from the at least one bi-directional FIFO.

47. The method of claim 42, further comprising the steps of:

Writing at least one fixed-length transmission unit to the second unidirectional FIFO buffer from the first unidirectional FIFO buffer using a first enabled diagnostic loop; and

Writing at least one fixed-length transmission unit to the first unidirectional FIFO buffer from the second unidirectional FIFO buffer over a second enabled diagnostic loop.

48. The method of claim 42, further comprising steps of:
 - outputting a write port fixed-length transmission unit count from each unidirectional FIFO buffer;
 - outputting a read port fixed-length transmission unit count from each unidirectional FIFO buffer; and
 - outputting from a read port of each unidirectional FIFO buffer a status indicating space available in the unidirectional FIFO buffer for at least one more fixed-length transmission unit.
49. The method of claim 42, wherein the plurality of ports comprise at least one asynchronous transfer mode (ATM) interface, at least one frame relay interface, at least one voice interface, at least one data interface, at least one network switch interface, at least one OC12 interface, and at least one OC3 interface.